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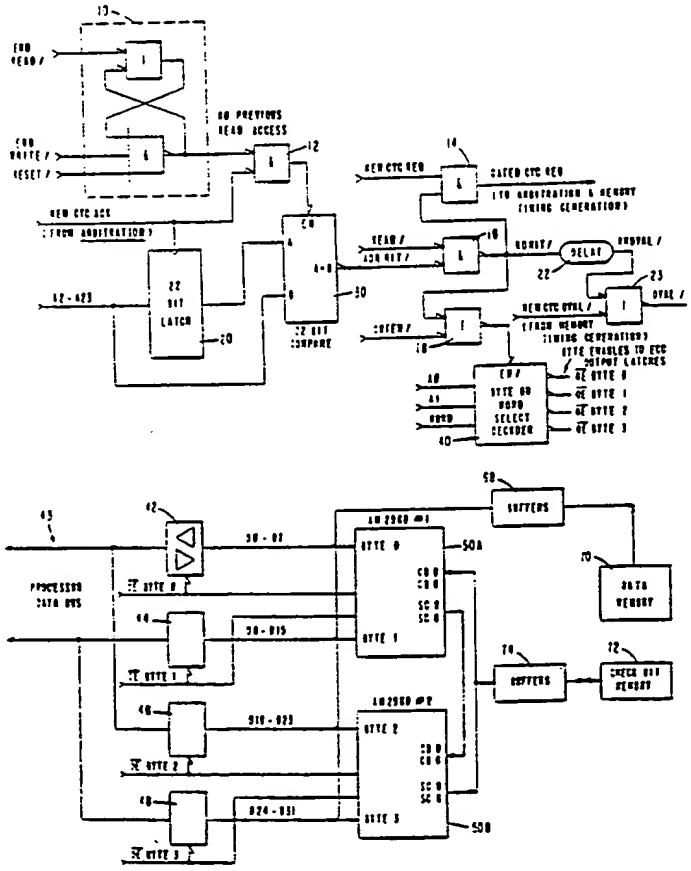
(54) Title: MEMORY ADDRESSING SYSTEM

(57) Abstract

A memory addressing system includes an addressable memory (70) provided with error checking and correction (ECC) circuits (50A, 50B) which include output latches (54B, 54D) adapted to latch corrected data read from the memory (70). An applied memory address is compared in a comparator (30) with a previous memory address stored in an address latch (20) and if a match is detected, a match signal is effective to inhibit the occurrence of the next memory cycle and to activate a decoder (40) coupled to the output of the ECC circuits (50A, 50B) to cause transfer to the system bus (43) of selected data from the ECC latches (54B, 54D). If no match is detected, a memory cycle is initiated to access the desired data in the memory (70). A high-speed memory operation is thus achieved utilizing simple circuitry.



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MEMORY ADDRESSING SYSTEM

Technical Field

This invention relates to memory addressing systems of the kind including an addressable memory, data storage means adapted to store data accessed from said memory for at least one memory cycle, address storage means adapted to receive and store an address corresponding to memory accessed data, and comparison means coupled to said address storage means and adapted to compare the stored address with a present memory address.

The invention has a particular application to memory addressing systems having error checking and correcting features.

Background Art

A memory addressing system of the kind specified is known from U.S. Patent Specification No. 4,156,905. According to the known system, an address having first and second portions is utilized to address a group of words from memory, using the first address portion. The group of words is stored in output registers and the second address portion is utilized to select particular words contained in the output registers. A number of second address portions may be used in any processor cycle. In order to access a subsequent group of words, a second first address portion is loaded into a pre-fetch register. The previously loaded first address portion is compared with the current first address portion to determine if they are the same. If they are, then the need for loading a group of words into the output registers is eliminated. If they are not the same, a miscomparison signal is generated to clock a new group of words into the output registers, utilizing the stored second first address portion.

The known system provides a high speed for memory access but has the disadvantage of complexity

resulting from the provision of a pre-fetch register and the consequent need to determine in advance the corresponding address portion of a group of words to be accessed in the future.

Disclosure of the Invention

It is an object of the present invention to provide a memory addressing system of the kind specified wherein the aforementioned disadvantage is alleviated.

Therefore, according to the present invention, there is provided a memory addressing system of the kind specified, characterized in that said comparison means is adapted to provide a match signal if a match exists, and by decoder means responsive to the provision of said match signal to enable the provision of memory accessed data stored in said data storage means.

It will be appreciated that a memory addressing system according to the immediately preceding paragraph is of simple construction and has the capability of operating in a manner compatible with the standard memory addressing mode, while providing pre-fetch operating capability.

It should be understood that in order to reduce memory overhead in memory systems with error checking and correction, a wide memory word is desirable. For a 256K byte system with double bit error detection and single bit error correction, implemented with 64K bit dynamic RAM, a total of 44 dynamic RAM devices are required if a 16 bit wide word is used, while only 39 dynamic RAM devices are required if a 32 bit word is used. In addition to requiring extra memory devices, error correcting memories are inherently slower than comparable width non-error correcting memories constructed from equivalent devices because of the checking time required for each read cycle. Further, if the memory word is wider than the processor data path, as is

desirable for reducing memory chip overhead, then all memory write cycles are required to be read-modify-write (R-M-W) cycles. R-M-W cycles take approximately twice the time to complete as simple write cycles on non-ECC memories and have an additional adverse impact on the performance of an ECC Memory System.

A memory address system according to the present invention can be applied to overcoming the performance degradation due to the 32 bit wide memory word. Performance for the 32 bit wide memory can be made greater than that for a 16 bit wide memory. Large scale integrated circuit (LSI) error correction devices (ECC's) can be cascaded for use in 32 bit wide memory systems. These error correcting devices have output data latches that store corrected data during memory read cycles, and these latches are individually addressable on a byte basis. Thus, four bytes, or two words, are stored on each memory read. Additional circuitry can be added to detect when the currently accessed byte or word is in the same four byte address space as the last read byte or word. When this condition is detected, the memory is not cycled since the data is already present at the output latches of the ECC devices. The addressed byte, or word, is enabled onto the data bus from the appropriate ECC output latches. The access time of the memory, as seen by the processor in this instance, is much shorter than that required by the fastest 16 bit MOS processors currently available.

Brief Description of the Drawings

One embodiment of the invention will now be described by way of example with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram, partially in logic level form, illustrating a first portion of the preferred embodiment of the invention:

Fig. 2 is a block diagram, partially in logic level form, illustrating a second portion of the preferred embodiment of the invention;

Fig. 3 is a block diagram, partially in logic level form, illustrating in more detail one of the blocks shown in Fig. 2; and

Fig. 4 illustrates the waveforms present at labeled points in the preferred embodiment of the invention.

Best Mode for Carrying Out the Invention

Referring to Fig. 1 in conjunction with the waveforms of Fig. 4, a latch 10 receives as its inputs the signals END READ, END WRITE and RESET. The latch's output is a signal labeled NO PREVIOUS READ ACCESS. The latch is cleared on power up, or system reset, by the RESET signal. At the end of each read cycle, the END READ signal sets the latch, indicating in a 32 bit system that four new bytes have been latched into the ECC's output latches (shown in Fig. 3). At the end of a write cycle, the signal END WRITE will clear the latch indicating that data in memory is different from the data in the ECC's output latches.

A 22 bit latch 20 receives as its inputs the 22 memory address bits, A2-A23. Additionally, there is provided a signal MEM CYC ACK. The MEM CYC ACK signal is active each time the memory is cycled. The latch 20 stores the accessed memory address bits upon being activated by the presence of the MEM CYC ACK signal. A 22 bit comparator 30 receives at its inputs the previous cycle's 22 address bits from the output of latch 20 and the 22 present address bits. The comparator compares each of these bits to determine if there is a match, if so the comparator, when enabled, will provide an output signal ADRHIT. In addition, the comparator is enabled by the output signal from an AND gate 12. The inputs to AND gate 12 are the output signal from the

latch 20 and the MEM CYC ACK signal. If the previous memory cycle was a READ, the output of AND gate 12 will be low and the output signal from the comparator 30 will be the address hit signal ADRHIT which goes active (low) indicating an access to the same four bytes that have previously been latched into the ECC device is presently requested. If the present cycle is a READ, a READ signal is addressed to the input of an AND gate 16 along with the ADRHIT signal. The output signal from AND gate 16 is the RD HIT signal which will go active (low). The output signal from AND gate 16 is directed as inputs to AND gate 14, delay element 22, and NAND gate 18. When the RD HIT signal is low, AND gate 14 will be inhibited from activating the gated cycle request signal, GATED CYC REQ, which appears at its output when a MEM CYC REQ input signal is present at its input. The GATED CYC REQ signal is directed to the data memory 70 (Fig. 2) and will initiate a memory cycle when an address hit is not detected. Instead, a decoder 40 will be enabled by the output signal from NAND gate 18, enabling signals $\overline{OE}$ BYTE Ø-3 to the respective gate latches 54 (Fig. 3) in the ECC device 50A and 50B (Fig. 2). The decoder 40, in the preferred embodiment, was a 2-to-4 decoder having the general TTL designation 74S139. The NAND gate 18 is enabled by the signal OUTEN which is a timing signal from memory. When enabled, the data corresponding to the addressed bytes is processed onto the computer system's data bus. The inputs A_0 and A_1 are the two low order address bits which constitute the byte select addresses. In addition, there is a WORD input which selects the word line. If the word line is active, it indicates a 16-bit transfer, that is, two bytes from the ECC output latches. The delay element 22, coupled to the output of the AND gate 16, allows time for data to be enabled onto the data bus. The signal RHDVAL/, indicates to the processor when data is valid after a read cycle. A NAND gate 23 receives the RHDVAL signal

and the MEM CYC DVAL/ signal to provide the signal DVAL/ which indicates valid data available independent of the type of cycle performed.

Referring now to Fig. 2, wherein the signals emanating from the decoder 40, denoted $\overline{OE}$ BYTE 0-3 are directed as enabling inputs to bidirectional drivers 42, 44, 46 and 48, respectively. In addition, each of these signals is directed to associated error checking and correcting code devices 50A and 50B which are identical in construction and which are shown in further detail in Fig. 3. The bidirectional drivers when enabled, in a first direction, pass information from the ECC devices 50A and 50B onto the processor data bus 43. When enabled in a second direction, data can pass from the processor bus to the ECC devices. A data memory 70 is coupled by means of buffers 68 to corresponding inputs of the ECC devices and to the processor data bus by means of the drivers. A check bit memory 72 is coupled to the ECC devices by means of buffers 74. In the preferred embodiment of the invention, the ECC units were 16 bit error detection and correction units identified by Part No. AM2960 manufactured by Advanced Micro Devices, Inc. which have the capability of being cascaded to form a 32 bit device.

In Fig. 3, there is disclosed, in block diagram form, one 16 bit ECC device. The error check and correction circuit 50A is shown comprised of a block of input latches 52, a block of output latches and buffers 54, a check bit generation circuit 58, which feeds a syndrome generator 60, a multiplexer 62, driver 64, and an error detection and correction logic circuit 56.

The input latches are shown consisting of three D-type flip-flops 52A-52C. The input bits to latch 52A are the signals CB0-CB6 derived from the cascaded error detection circuit 50B. The inputs to the latch 52B are the data bits D0-D7. The inputs to the latch 52C are the data bits D8-D15. Each of the input

latches 52 are enabled by the signal LE IN. When the signal LE IN is high the signal present on the input of the latches passes through the latches. When the signal LE IN makes a transition from high-to-low the data present on the inputs are latched to the outputs. The outputs from latches 52B and 52C are directed as inputs to the error detection and correction logic circuit 56 and to the check bit generation circuit 58. The data bits D_0-D_{15} received by the error detection and correction logic are checked and corrected if a single bit error exists. The correct data bits D_0-D_7 and D_8-D_{15} are directed to the D inputs of output latches 54B and 54D, respectively. The signal LE OUT applied to latches 54B and 54D controls the latches similar to the signal LE IN except that the LE OUT signal activates the latches 54B and 54D shortly after the input latches 52 are activated to permit the data received by the input latches, and error checked by the error detection and correction logic 56, to be passed back to the processor bus. The outputs of latches 54B and 54D are directed as inputs to output buffers 54A and 54C respectively. These output buffers are enabled by the $\overline{OE}$ BYTE 0 and $\overline{OE}$ BYTE 1 signals, respectively. The output buffers are coupled to the corresponding input-output lines labeled D_0-D_7 and D_8-D_{15}.

In operation then, when the data bits appearing at the output of the error detection and correction logic circuit are certain to be the bits associated with the address that is next desired by the processor, the output buffers are enabled and the data bits are passed on to the data bus. Check bit generation and syndrome bit generation is well-known in the art and is not discussed in further detail. The multiplexer 62 activated by the level of the signal at the output of latch 52A directs the output of the syndrome generator to driver 64 which, upon receiving an enabling signal, $\overline{OE}$ SC, provides the syndrome bits SC0-SC6 at its output

which syndrome bits are coupled to the associated ECC unit 50B. When the signal $\overline{OE}$ SC is high partial syndrome bits are passed from the ECC element 50B to the ECC element 50A. When the signal $\overline{OE}$ SC goes from high to low all of the syndrome bits are made available to the buffer 74 and check bit memory 72. The error checking and correction logic circuit additionally performs its basic function of providing an output signal $\overline{ERROR}$ indicative of a single error, which error has been corrected or an output signal $\overline{MULT\ ERROR}$ which indicates the existence of a multi-error, in which case the error is not correctable by the correction logic 56.

Referring now to Fig. 4, wherein the timing waveforms associated with the operation of the preferred embodiment are shown. During cycle 1, assuming the previous cycle was a write cycle, and that the error correction circuit did not contain valid data. The memory is cycled and a 32 bit word at location 8000 HEX (bytes 8000-8003) is latched into the input latches on the falling edge of the signal LE IN. The processor is requesting two bytes since WORD is active, so $\overline{OE}$ byte 0 and $\overline{OE}$ byte 1 are enabled and steered onto the processor data bus. In cycle 2, operation is another word read by the processor requesting bytes 8002 and 8003, which are already stored in the error checking and correction logic 56. The memory cycle is inhibited and signals $\overline{OE}$ byte 2 and $\overline{OE}$ byte 3 enable these two bytes onto the data bus. This cycle is substantially shorter than cycle 1, since memory is not accessed.

Signal Definitions:

CB0-CB7 - Check bit inputs from memory

SC0-SC7 - Check bit outputs on write cycles or syndrome outputs on read cycles

D0-D7 - Bi-directional data to/from memory (byte Ø)

D8-D15 - Bi-directional data to/from memory (byte 1)

LEIN - Latch control for check bit and data input latches

$\overline{OE}$SC - Output control for syndrome check bit driver
LEOUT - Latch control for data output latches (both byte Ø and byte 1)
$\overline{OE}$ BYTE Ø - Output control for byte Ø output buffer
$\overline{OE}$ BYTE 1 - Output control for byte 1 output buffer

Note: Two AM2960 devices are cascaded for the 32-bit memory system in which this prefetch logic is used. $\overline{OE}$ BYTE 2 refers to the output control for the lower byte (D16-D23) in the second AM2960, while $\overline{OE}$ BYTE 3 refers to the upper byte (D24-D31) in the second AM2960.

CLAIMS:

1. A memory addressing system including an addressable memory (70), data storage means (50A, 50B) adapted to store data accessed from said memory for at least one memory cycle, address storage means (20) adapted to receive and store an address corresponding to memory accessed data, and comparison means (30) coupled to said address storage means (20) and adapted to compare the stored address with a present memory address, characterized in that said comparison means (30) is adapted to provide a match signal if a match exists, and by decoder means (40) responsive to the provision of said match signal to enable the provision of memory accessed data stored in said data storage means (50A, 50B).

2. A memory addressing system according to claim 1, characterized by memory cycle control means (14) adapted to inhibit the initiation of a memory access cycle in response to the provision of said match signal.

3. A memory addressing system according to claim 1, characterized in that said data storage means is included in error checking and correction means (50A, 50B).

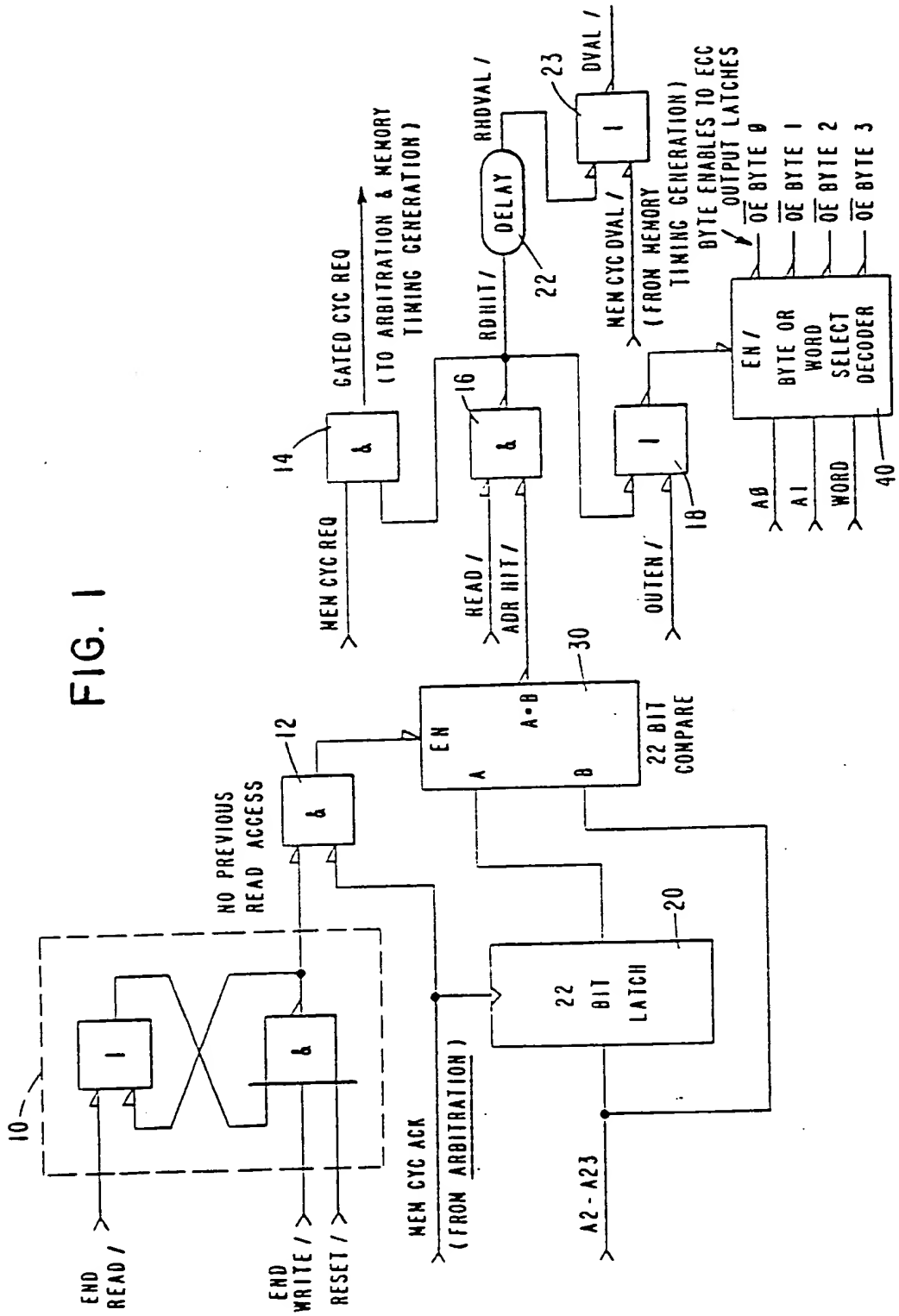
4. A memory addressing system according to claim 1, characterized by latching means (10) responsive to signals indicative of memory read and write cycles and adapted to provide an enabling signal to said comparison means (30) when the previous memory cycle was a read cycle.

5. A memory addressing system according to claim 1, characterized by logic means (16, 18) coupling said comparison means (30) to said decoder means (40) and adapted to receive a signal indicative of a memory

5. (concluded)
read cycle and to enable said decoder means (40) when said comparison means (30) provides said match signal in conjunction with a memory read cycle.

6. A memory addressing system according to claim 1, characterized by driver means (42-48) adapted to couple outputs of said data storage means (50A, 50B) to a system bus (43).

FIG. 1



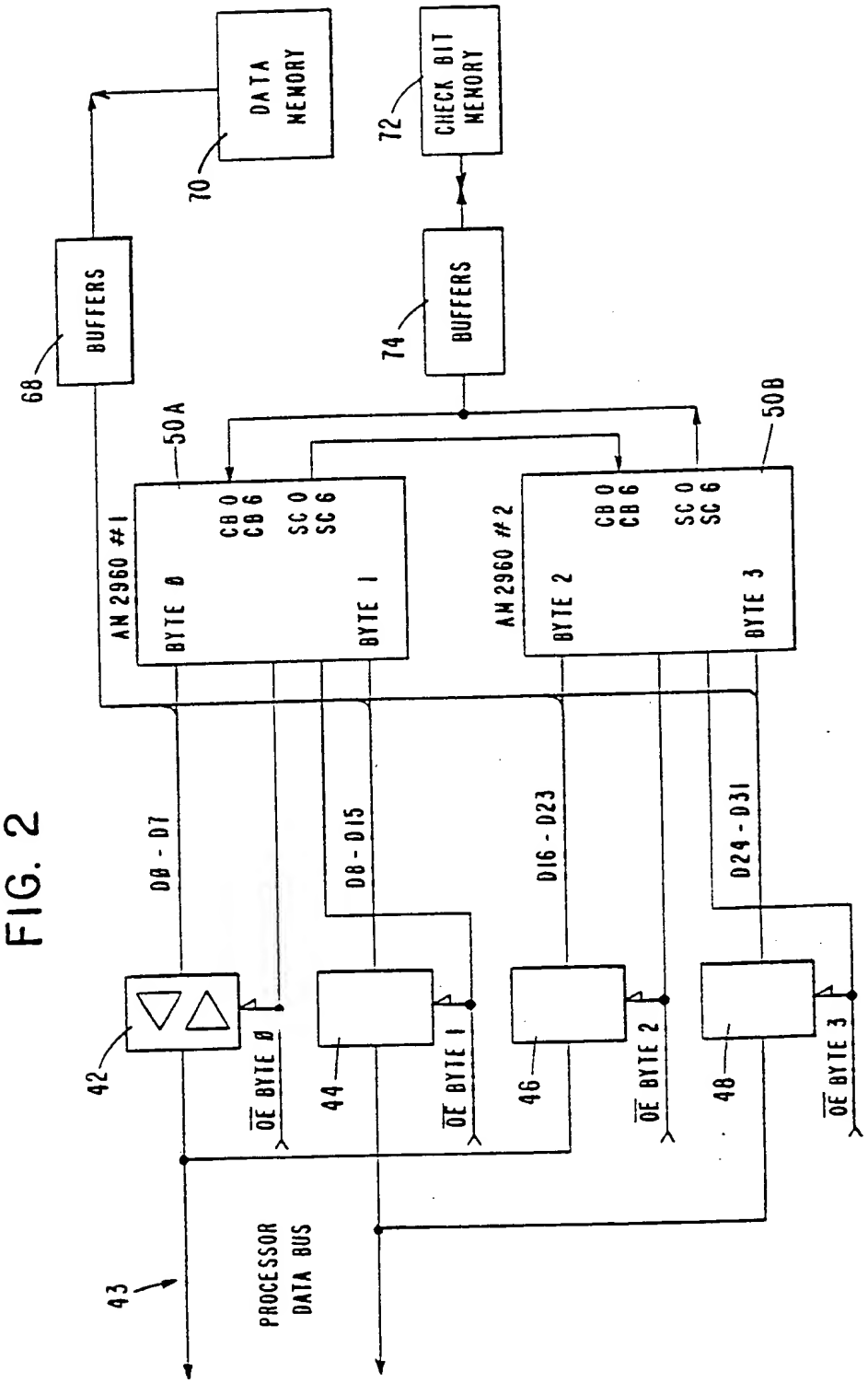


FIG. 2

FIG. 3

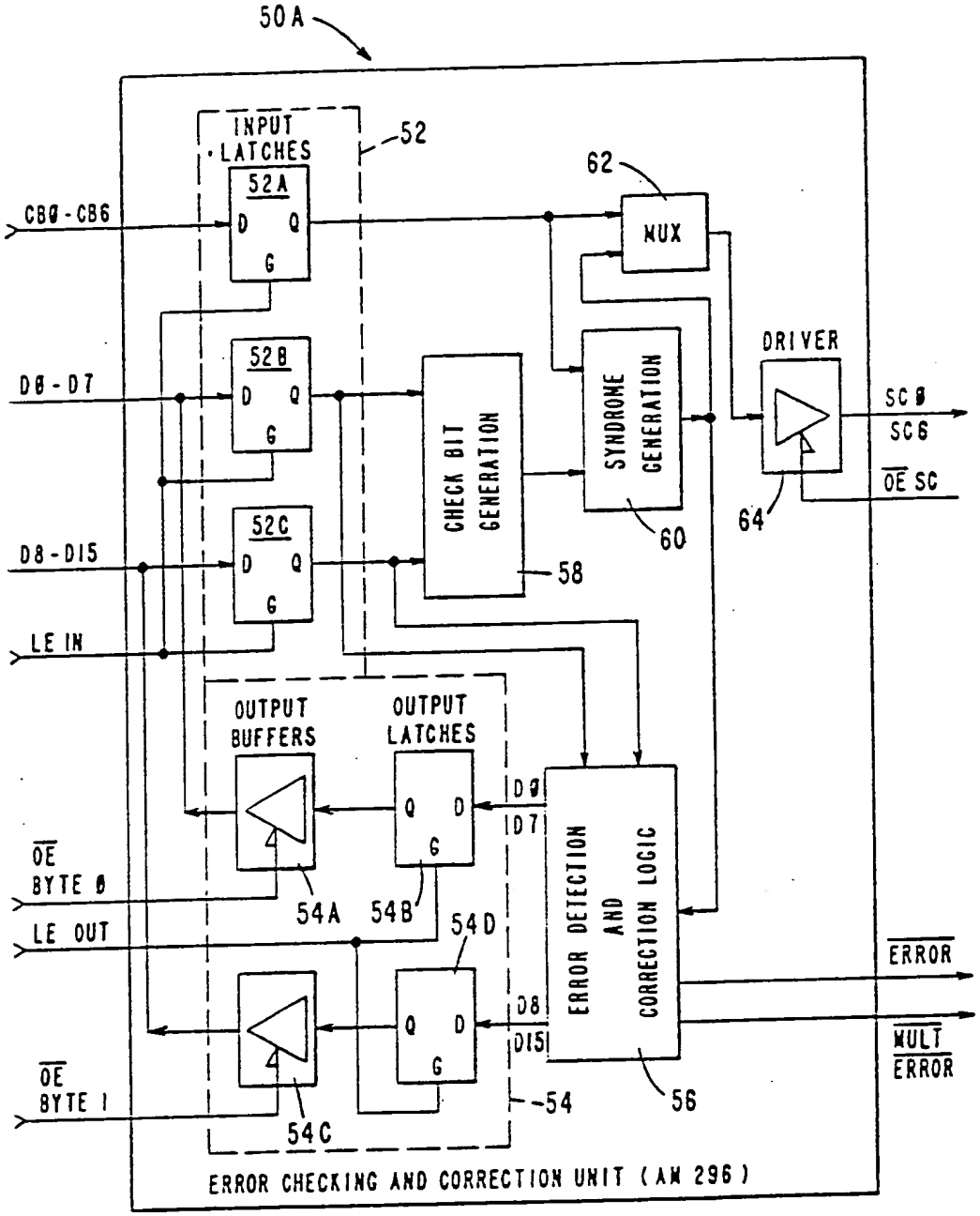
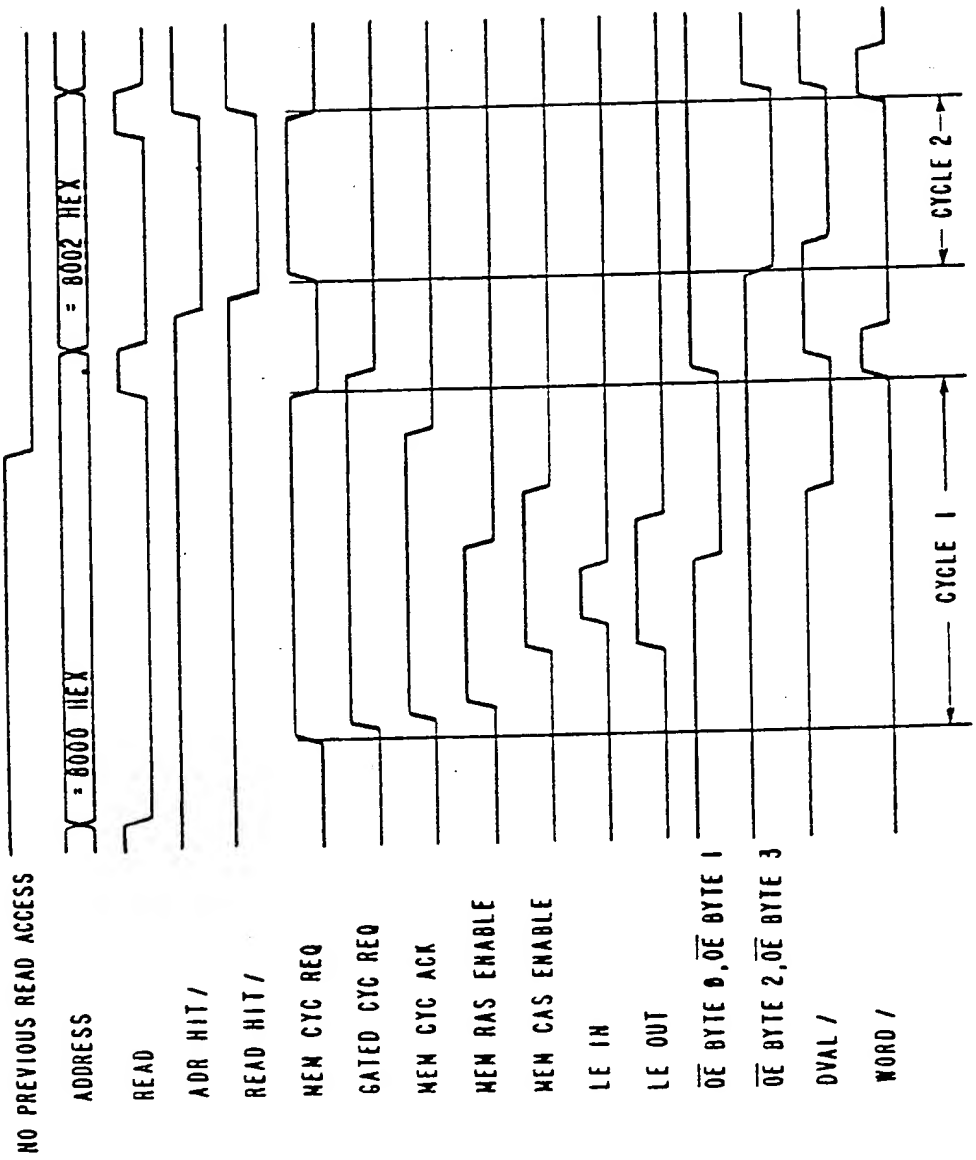


FIG. 4



INTERNATIONAL SEARCH REPORT

International Application No PCT/US 83/00710

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[3]: G 11 C 9/06

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC[3]	G 11 C 9/06; G 06 F 13/00

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
Y	Navy Technical Disclosure Bulletin, volume 4, no. 8, August 1979, Arlington (US) Wilcox: "Block parallel access memory", pages 43-48, see especially figures 1a, 1b; page 45, lines 1-8; page 46, lines 7-15; page 47, last paragraph - page 48, first paragraph	1-3
Y	US, A, 4292674 (SCHEUNEMAN) 29 September 1981, see figure 1, column 4, line 63 - column 5, line 7	1-3
P	Electronics International, volume 55, no. 16, 11 August 1982, New York (US) Knudsen: "Supermini goes multiprocessor route to put it up front in performance", pages 112-117, see especially page 116, right-hand column, lines 11-18	1,4,5
A	US, A, 4156905 (FASSBENDER) 29 May 1979 (cited in the application)	1

* Special categories of cited documents: [15]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
8th August 1983	30 AOUT 1983
International Searching Authority [1]	**Signature of Authorized Officer [20]**
EUROPEAN PATENT OFFICE	G.L.M. Kampenberg

Form PCT/ISA/210 (second sheet) (October 1981)

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 83/00710 (SA 5271)

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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A- 4292674	29/09/81	None		
US-A- 4156905	29/05/79	FR-A-	2401460	23/03/79
		GB-A-	2003302	07/03/79
		DE-A-	2836873	08/03/79
		JP-A-	54043625	06/04/79

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